

ABSTRACT OF THE DISCLOSURE

A memory device includes address bus termination circuitry that can be enabled or disabled depending on the state of an address bus termination control signal. A memory module may be made up of several of these memory devices with each memory device including address bus termination circuitry. The memory devices may be coupled to an address bus in a daisy chain configuration. In the case of a daisy chain configuration it may be desirable to only enable the address bus termination circuitry of the last memory device in the chain. The address bus termination circuitry of the last memory device in the chain can be enabled by tying its address bus termination control signal to a positive voltage. The address bus termination control signals of the other memory devices can be tied to ground in order to disable their address bus termination circuitry.